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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,623	07/02/2004	Andrew MG Westcott	540-508	2994

23117 7590 07/24/2008

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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	PAPER NUMBER
2836	
MAIL DATE	DELIVERY MODE
07/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,623	WESTCOTT, ANDREW MG	
	Examiner	Art Unit	
	CARLOS AMAYA	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,9-11 and 13-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6, 9-11, 13-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amendments filed on 4/8/2008.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,6, 9-11,13-15,17-25,28,30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Wilcox (US 5,847,554).

With respect to claims 1, 6 Dyer discloses a switching circuit, responsive to a voltage demand signal, for controlling current supplied to an inductor from a direct (DC) supply voltage, said switching circuit comprising a bridge circuit (see figure 1), said bridge circuit comprising: an input operable to receive a direct current, DC (bank battery 7), supply of nominal voltage +VS (battery 7 supplies the voltage for the input), an output, said output having opposed ends (outputs are generated at opposed end points A and B); first and second bride arms, said arms having corresponding first and second switches (Switches 21 and 19 of first and second arms respectively connected to opposed ends to the output) operable in response to first and second switching signals to be switched between on and off states (controller 29 in conjunction with driver circuits 31 and 32 supplies the signal for the switches to turn on and off, column 4 lines 24-37),

wherein switching between various combinations of on and off states produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally +VS, 0V and -VS (The turning on and off of the transistor produces a desired output as can be better seen in figure 3); controller 29 generates a signal to control the operation of the switches according to a demand signal.

Dyer, however, does not disclose expressly a voltage sensor for producing a signal indicative of said DC supply voltage; and a switching signal generator, responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals.

Wilcox discloses voltage sensing circuit 320 for sensing the voltage drop of the transistor, which is an indication of the current supplied by the regulator and the DC input Vin, see abstract. Figure 3 shows oscillator 104, latch 106, drivers 108 and 112, and sensing circuit 320 to control the switching signals provided to switches 342 and 344.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Dyer with the voltage sensor disclosed by Wilcox, col. 5 lines 1-42.

The suggestion or motivation for doing so would have been to avoid dissipative losses in current sensing elements and costly manufacturing process, col. 5 lines 37-42.

With respect to claims 9-11 Dyer in view of Wilcox disclose the switching circuit according to claim 1. Dyer discloses that the bridge circuit is a half-bridge with third and fourth arms having diodes (Column 3 lines 40-41, line 45). The first and second

switches are transistors (Transistor switching device 19 and 21). Comprising an electromagnet connected across the output of the bridge circuit (Figure 1 Inductor 5).

With respect to claim 13 Dyer discloses a method of operating a switching circuit comprising an input that receives a DC supply of nominal voltage +Vs (input voltage provided by the battery bank 11), an output (the output is provided to the load 5) and first and second switches (switches 19 and 21), the method comprising the steps of: (a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output in a period (controller 29 receives a demand signal, which is an indication of a desired output voltage, column 4 lines 24-37, also as shown in figure 3 the load voltage VL is applied to the load in a periodic fashion); (b) generating first and second switching signals with reference to the voltage demand signal (column 4 lines 24-27, the controller generates the signals to turn the switches on to generate the desired output voltage, with reference to the demand signal and with a reference to the shunt voltage); and (c) applying the first and second switching signals to the first and second switches respectively during the period (column 5 lines 17-25); wherein the switching signals cause the switches to switch between on and off states, switching between various combinations of on and off states of the first and second switches producing an electrical signal at the output with voltage pulses at levels of nominally +Vs, 0V and –Vs (column 6 lines 60-68, column 7 lines 1-13), the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the output during the period is substantially equal to the desired voltage (column 6 lines 7-12).

Dyer, however, does not disclose generating signals with reference to an indication of the DC supply voltage.

Wilcox discloses voltage sensing circuit 320 for sensing the voltage drop of the transistor, which is an indication of the current supplied by the regulator and the DC input Vin, see abstract.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Dyer with the voltage sensor disclosed by Wilcox, col. 5 lines 1-42.

The suggestion or motivation for doing so would have been to avoid dissipative losses in current sensing elements and costly manufacturing process, col. 5 lines 37-42.

With respect to claim 14 Dyer in view of Wilcox disclose the method of claim 13, wherein at least one of the first and second switching signals is generated with reference to a voltage signal indicative of the DC supply such that the at least one first or second switching signal compensates for fluctuations in the DC supply (as shown in figure 1 measurement device 27 is connect in series to a load to develop a signal proportional to the load this signal is in turned fed to a controller 29 and is compared with a demand signal and generates signals to control conduction of the switches, column 4 lines 20-37).

With respect to claim 15 Dyer in view of Wilcox disclose the method of claim 14, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply (the voltage signal from the bridge is pass through inductors 13 and 15 that act as a low-pass filter, column 3 lines 15-22).

With respect to claim 17 Dyer in view of Wilcox discloses the method of claim 13, wherein at least one of the first and second switching signals is generated to compensate for a voltage drop across a diode and/or transistor in the switching circuit. Wilcox discloses a sensing circuitry 320 to sense the voltage drop across the switching elements, and in turn compensates for this voltage drop to vary the duty cycle of the regulator, Column 4 lines 57-60.

With respect to claim 18 Dyer in view of Wilcox disclose the method of claim 17, wherein the at least one of the first and second switching signals is generated with reference to a current signal indicative of the current flowing through the output and a representative resistance of the diode transistor (column 4 lines 57-67).

With respect to claim 19 Dyer in view of Wilcox disclose the method of claim 13, wherein at least one of the first or second switching signals is generated with reference to a measure of a voltage offset caused by a slow response in generating the first or second switching signals. As disclosed by Wilcox depending on the voltage drop sense/offset the duty cycle is change to supply the correct power by the regulator.

With respect to claim 20 Dyer in view of Wilcox disclose the method of claim 13, wherein the switching circuit comprises a bridge circuit having an input that receives the DC supply signal of voltage, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output, this limitation is disclosed by the method of claim 13.

With respect to claim 21 Dyer in view of Wilcox disclose the method of claim 20 Dyer discloses that the bridge circuit is a half-bridge with third and fourth arms having diodes (Column 3 lines 40-41, line 45).

With respect to claim 22 Dyer in view of Wilcox disclose the method of claim 20, wherein the first and second switches are transistor and the method comprises the step of switching the transistors between on and off states corresponding to substantially minimum voltage drop and substantially minimum current flow, respectively, through the transistors. Wilcox discloses a voltage drop sensing circuitry, corresponding to a minimum voltage drop (Column 7 lines 1-4, and 10-17) and substantially minimum current flow respectively through the transistor (figure 1 shows a current mode synchronous step-down switching regulator 100, by sensing a current minimum/maximum). (Regulator 900 by way of the PWM 912 controls the operation of the transistor between minimum values. Figure 10, Column 7 lines 22-25). Figure 9 shows the circuit of figure 3 with the only difference being the sensing circuitry 920 and the inverter 910.

With respect to claim 23 Dyer in view of Wilcox disclose the method according to claim 13 comprising the step of generating pulsed first and second signals (figure 1 shows the controller 29 in conjunction with drivers 31 and 33 generates a first and second pulsed signals for the first and second switches).

With respect to claim 24 Dyer in view of Wilcox disclose the method according to claim 23 comprising the step of generating the first and second switching signals according to a rule that the first and second switches are not switched concurrently

(column 6 lines 60-68, column 7 lines 1-13, shows that depending on a desired output the switches are controlled accordingly).

With respect to claim 25 Dyer in view of Wilcox disclose the method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the signals are to have no more than one pulse per period (Column 5 lines 17-25).

With respect to claim 28 Dyer in view of Wilcox disclose the method of claim 23 comprising the step of generating the first and second switching signals according to a pulse width modulation scheme (column 4 lines 56-63, also as shown in figure 3).

With respect to claim 30 Dyer in view of Wilcox disclose the method of claim 13 comprising the step of receiving a current demand signal (demand signal figure 1) indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output during a period (Column 4 lines 3-6, output being control by controller 29 and timing circuits) that results in the electrical signal being supplied to the output during the period with a current substantially equal to the desired current (controller 29 controls the operation of transistors 19 and 21 to produce at the load an output current substantially equal to a desired current, column 6 lines 2-12).

With respect to claim 31-32 Dyer in view of Wilcox disclose the method of claim 30, the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output. Further comprising

the step of generating the voltage demand signal with reference to a current signal indicative of a current flowing through the output (Column 4 lines 22-30).

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Wilcox (US 5,847,554) in further view of Durif (US 6,504,698).

With respect to claim 16 Dyer and Wilcox disclose the method of claim 15, except that the voltage signal is passed through a finite impulse response filter.

Durif discloses the measurement of input voltages comprising FIR, column 1 lines 49-53, and column 7 lines 14-17, 50-67.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a FIR filter disclosed by Durif in the filter disclosed by Dyer and Wilcox to measure the fluctuation in the DC supply.

The suggestion or motivation for doing so would have been to obtain a more accurate reading of the input voltage fluctuations by using the FIR filter.

5. Claims 26, 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Wilcox (US 5,847,554) in further view of Ramarathnam (US 6,316,895)

With respect to claim 26 Dyer and Wilcox disclose the method of claim 23, however, does not disclose that the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period. Ramarathnam, however, discloses in figure 8 that the pattern of

the switching signals is symmetric with respect to the center of the switching period (Column 7 lines 62-67).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to perform the step of generating the signals in a symmetric manner with respect to the period as disclosed by Ramarathnam in dyer and Wilcox's invention.

The suggestion or motivation for doing so would have been to obtain an output signal free of distortions and provide a required output to a load as precise as possible. Ramarathnam teaches that the symmetric PWM is used to produce least harmonics at the output.

With respect to claims 33 and 34 Dyer in view of Wilcox disclose the method of claim 13, however, does not disclose a computer program comprising program code means for performing the method steps of claim 13 when the program is run on a computer associated with the switching circuit. Ramarathnam discloses a software program to control the operation of the switches (Column 3 lines 20-27 and lines 66-67). Dyer does not disclose a computer program product stored on a computer readable medium. Ramarathnam discloses a micro-controller (5) with a ROM and RAM, and the software program being installed in the ROM (Column 6 lines 29-36).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to have a computer program and a computer program product with storing means performed the steps of the invention disclosed by Dyer.

The suggestion or motivation for doing so would have been to obtain a more precise output voltage with the sensing circuitry of Dyer, since a computer and computer codes are controlling the voltage generated by the switching circuitry.

6. Claims 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Wilcox (US 5,847,554) in further view of Smedley (US 5,559,467).

With respect to claim 29, Dyer and Wilcox disclose the method of claim 23, except for the step of noise shaping the first and second switching signals. Smedley, however, discloses a noise shaper 60 operable to noise-shape the first and second signals produced by the PWM 64 (Figure 4 lines 34-37).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art, to insert a noise shaper as described by Smedley in the switching circuit of Dyer.

The suggestion or motivation for doing so would have been to produce a signal free of noise, to obtain a more reliable operation of the switches that is factored into a better supply of power to the load.

7. Claims 1,6, 9-11,13-15,17-18, 20-21,23-25,28,30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Kern (US 6,081,104).

With respect to claims 1, 6 Dyer discloses a switching circuit, responsive to a voltage demand signal, for controlling current supplied to an inductor from a direct (DC)

supply voltage, said switching circuit comprising a bridge circuit (see figure 1), said bridge circuit comprising: an input operable to receive a direct current, DC (bank battery 7), supply of nominal voltage +VS (battery 7 supplies the voltage for the input), an output, said output having opposed ends (outputs are generated at opposed end points A and B); first and second bride arms, said arms having corresponding first and second switches (Switches 21 and 19 of first and second arms respectively connected to opposed ends to the output) operable in response to first and second switching signals to be switched between on and off states (controller 29 in conjunction with driver circuits 31 and 32 supplies the signal for the switches to turn on and off, column 4 lines 24-37), wherein switching between various combinations of on and off states produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally +VS, 0V and -VS (The turning on and off of the transistor produces a desired output as can be better seen in figure 3); controller 29 generates a signal to control the operation of the switches according to a demand signal.

Dyer, however, does not disclose expressly a voltage sensor for producing a signal indicative of said DC supply voltage; and a switching signal generator, responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals.

Kern discloses a DC input voltage sensor 58 for sensing the input voltage and producing a signal to a controller 82; controller 82 in turn produces a signal to control the switches of the power converter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the invention disclosed by Dyer to include the voltage sensor 58 to supply a signal indicative of the DC supply, for the purpose of obtaining a desired output based on the available supply (col. 7 lines 42-47).

With respect to claims 9-11 Dyer in view of Kern disclose the switching circuit according to claim 1. Dyer discloses that the bridge circuit is a half-bridge with third and fourth arms having diodes (Column 3 lines 40-41, line 45). The first and second switches are transistors (Transistor switching device 19 and 21). Comprising an electromagnet connected across the output of the bridge circuit (Figure 1 Inductor 5).

With respect to claim 13 Dyer discloses a method of operating a switching circuit comprising an input that receives a DC supply of nominal voltage +Vs (input voltage provided by the battery bank 11), an output (the output is provided to the load 5) and first and second switches (switches 19 and 21), the method comprising the steps of: (a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output in a period (controller 29 receives a demand signal, which is an indication of a desired output voltage, column 4 lines 24-37, also as shown in figure 3 the load voltage VL is applied to the load in a periodic fashion); (b) generating first and second switching signals with reference to the voltage demand signal (column 4 lines 24-27, the controller generates the signals to turn the switches on to generate the desired output voltage, with reference to the demand signal and with a reference to the shunt voltage); and (c) applying the first and second switching signals to the first and second switches respectively during the period (column 5 lines 17-25); wherein the

switching signals cause the switches to switch between on and off states, switching between various combinations of on and off states of the first and second switches producing an electrical signal at the output with voltage pulses at levels of nominally +Vs, 0V and –Vs (column 6 lines 60-68, column 7 lines 1-13), the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the output during the period is substantially equal to the desired voltage (column 6 lines 7-12).

Dyer, however, does not disclose generating signals with reference to an indication of the DC supply voltage.

Kern discloses a DC input voltage sensor 58 for sensing the input voltage and producing a signal to a controller 82; controller 82 in turn produces a signal to control the switches of the power converter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the invention disclosed by Dyer to include the voltage sensor 58 to supply a signal indicative of the DC supply, for the purpose of obtaining a desired output based on the available supply (col. 7 lines 42-47).

With respect to claim 14 Dyer in view of Kern disclose the method of claim 13, wherein at least one of the first and second switching signals is generated with reference to a voltage signal indicative of the DC supply such that the at least one first or second switching signal compensates for fluctuations in the DC supply (as shown in figure 1 measurement device 27 is connect in series to a load to develop a signal proportional to the load this signal is in turned fed to a controller 29 and is compared

with a demand signal and generates signals to control conduction of the switches, column 4 lines 20-37).

With respect to claim 15 Dyer in view of Kern disclose the method of claim 14, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply (the voltage signal from the bridge is pass through inductors 13 and 15 that act as a low-pass filter, column 3 lines 15-22).

With respect to claim 17 Dyer in view of Kern disclose the method of claim 13, wherein at least one of the first and second switching signals is generated to compensate for a voltage drop across a diode and/or transistor in the switching circuit (Kern's controller 82 compensate for the voltage drop across the transistor 128 by controlling the duty cycle of the switch, col. 9 lines 18-37).

With respect to claim 18 Dyer in view of Kern disclose the method of claim 17, wherein the at least one of the first and second switching signals is generated with reference to a current signal indicative of the current flowing through the output and a representative resistance of the diode transistor. Controller 82 receives signals from current sensors 90 and 92, which monitor the output voltage and controls the switches accordingly.

With respect to claim 20 Dyer in view of Kern disclose the method of claim 13, wherein the switching circuit comprises a bridge circuit having an input that receives the DC supply signal of voltage, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output, this limitation is disclosed by the method of claim 13.

With respect to claim 21 Dyer in view of Kern disclose the method of claim 20 Dyer discloses that the bridge circuit is a half-bridge with third and fourth arms having diodes (Column 3 lines 40-41, line 45).

With respect to claim 23 Dyer in view of Kern disclose the method according to claim 13 comprising the step of generating pulsed first and second signals. Kern discloses that controller 82 provides a PWM logic signal to control the switches.

With respect to claim 24 Dyer in view of Kern disclose the method according to claim 23 comprising the step of generating the first and second switching signals according to a rule that the first and second switches are not switched concurrently (column 6 lines 60-68, column 7 lines 1-13, shows that depending on a desired output the switches are controlled accordingly).

With respect to claim 25 Dyer in view of Kern disclose the method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the signals are to have no more than one pulse per period (Column 5 lines 17-25).

With respect to claim 28 Dyer in view of Kern disclose the method of claim 23 comprising the step of generating the first and second switching signals according to a pulse width modulation scheme (column 4 lines 56-63, also as shown in figure 3); Kern discloses that controller 82 provides a PWM logic signal to control the switches.

With respect to claim 30 Dyer in view of Kern disclose the method of claim 13 comprising the step of receiving a current demand signal (demand signal figure 1) indicative of a desired current to be supplied to the output in a period and calculating the

voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output during a period (Column 4 lines 3-6, output being control by controller 29 and timing circuits) that results in the electrical signal being supplied to the output during the period with a current substantially equal to the desired current (controller 29 controls the operation of transistors 19 and 21 to produce at the load an output current substantially equal to a desired current, column 6 lines 2-12).

With respect to claim 31-32 Dyer in view of Kern disclose the method of claim 30, the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output. Further comprising the step of generating the voltage demand signal with reference to a current signal indicative of a current flowing through the output (Column 4 lines 22-30).

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Kern (US 6,081,104) in further view of Durif (US 6,504,698).

With respect to claim 16 Dyer and Kern disclose the method of claim 15, except that the voltage signal is passed through a finite impulse response filter.

Durif discloses the measurement of input voltages comprising FIR, column 1 lines 49-53, and column 7 lines 14-17, 50-67.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a FIR filter disclosed by Durif in the filter disclosed by Dyer and Kern to measure the fluctuation in the DC supply.

The suggestion or motivation for doing so would have been to obtain a more accurate reading of the input voltage fluctuations by using the FIR filter.

9. Claims 26, 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Kern (US 6,081,104) in further view of Ramarathnam (US 6,316,895)

With respect to claim 26 Dyer and Kern disclose the method of claim 23, however, does not disclose that the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period. Ramarathnam, however, discloses in figure 8 that the pattern of the switching signals is symmetric with respect to the center of the switching period (Column 7 lines 62-67).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to perform the step of generating the signals in a symmetric manner with respect to the period as disclosed by Ramarathnam in dyer and Kern's invention.

The suggestion or motivation for doing so would have been to obtain an output signal free of distortions and provide a required output to a load as precise as possible. Ramarathnam teaches that the symmetric PWM is used to produce least harmonics at the output.

With respect to claims 33 and 34 Dyer in view of Kern disclose the method of claim 13, however, does not disclose a computer program comprising program code means for performing the method steps of claim 13 when the program is run on a

computer associated with the switching circuit. Ramarathnam discloses a software program to control the operation of the switches (Column 3 lines 20-27 and lines 66-67). Dyer does not disclose a computer program product stored on a computer readable medium. Ramarathnam discloses a micro-controller (5) with a ROM and RAM, and the software program being installed in the ROM (Column 6 lines 29-36).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to have a computer program and a computer program product with storing means performed the steps of the invention disclosed by Dyer and Kern.

The suggestion or motivation for doing so would have been to obtain a more precise output voltage with the sensing circuitry of Dyer, since a computer and computer codes are controlling the voltage generated by the switching circuitry.

10. Claims 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer (US 4,585,986) in view of Kern (US 6,081,104) in further view of Smedley (US 5,559,467).

With respect to claim 29, Dyer and kern disclose the method of claim 23, except for the step of noise shaping the first and second switching signals. Smedley, however, discloses a noise shaper 60 operable to noise-shape the first and second signals produced by the PWM 64 (Figure 4 lines 34-37).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art, to insert a noise shaper as described by Smedley in the switching circuit of Dyer and Kern.

The suggestion or motivation for doing so would have been to produce a signal free of noise, to obtain a more reliable operation of the switches that is factored into a better supply of power to the load.

Response to Arguments

11. Applicant's arguments filed 4/8/2008 have been fully considered but they are not persuasive.

It is respectfully submitted that Wilcox discloses a Vds sensing circuitry 320 for measuring the voltage drop of the transistors, which as shown in figure 3 is a clear indication of Vin; col. 5 lines 1-42, disclose that Vds sensing circuitry **combines** the current sensed from the drain-to -source voltage measurements (which is and indication of Vin) and the inductor current the claim calls for "a voltage sensor for producing a signal indicative of said DC supply voltage".

With respect to the argument of the motivation for combining the two references, it is respectfully submitted that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re Mclaughlin, 170 USPQ 209 (CCPA 1971) references are evaluated by what

they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

PLEASE NOTE: Error #5 in pre-Appeal brief dated 6/15/2007 is in Error, 35 USC 103 (c) ONLY applies to prior art rejections NOT Double Patent Rejections.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1, 13-20, 23-34 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 7,187,567. Although the conflicting claims are not identical, they are not patentably distinct from each other because.

With respect to claims 1, claim 27 of Patent (US 7,187,567) discloses the limitations of claims 1 and 13.

With respect to claim 14, claim 12 of Patent (US 7,187,567) disclose the limitations of claim 14.

With respect to claim 15, claim 13 of Patent (US 7,187,567) disclose the limitations of claim 15.

With respect to claim 16, claim 14 of (US 7,187,567) discloses the switching circuit as claimed in claimed 16.

With respect to claim 17, claim 15 of (US 7,187,567) discloses the switching. circuit as claimed in claimed 17.

With respect to claim 18, claim 16 of (US 7,187,567) discloses the switching circuit as claimed in claimed 18.

With respect to claim 19, claim 17 of (US 7,187,567) discloses the switching circuit as claimed in claimed 19.

With respect to claim 20, claim 25 of (US 7,187,567) discloses the switching circuit as claimed in claimed 20.

With respect to claim 23, claim 2 of (US 7,187,567) discloses the switching circuit as claimed in claimed 23.

With respect to claim 24, claim 3 of (US 7,187,567) discloses the switching circuit as claimed in claimed 24.

With respect to claim 25, claim 4 of (US 7,187,567) discloses the switching circuit as claimed in claimed 25.

With respect to claim 26, claim 5 of (US 7,187,567) discloses the switching circuit as claimed in claimed 26.

With respect to claim 27, combination of claims 2-6 of (US 7,187,567) discloses the switching circuit as claimed in claimed 27.

With respect to claim 28, claim 7 of (US 7,187,567) discloses the switching circuit as claimed in claimed 28.

With respect to claim 29, claim 18 of (US 7,187,567) discloses the switching circuit as claimed in claimed 29.

With respect to claim 30, claim 20 of (US 7,187,567) discloses the switching circuit as claimed in claimed 30.

With respect to claim 31, claim 1 of (US 7,187,567) discloses the switching circuit as claimed in claimed 31.

With respect to claim 32, claim 1 of (US 7,187,567) discloses the switching circuit as claimed in claimed 31.

With respect to claim 33, claim 23 of (US 7,187~567) discloses the switching circuit as claimed in claimed 33.

With respect to claim 34, claim 24 of (US 7,187,567) discloses the switching circuit as claimed in claimed 33.

14. Claims 1, 13-20, 23-34 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 7,348,689. Although the conflicting claims are not identical, they are not patentably distinct from each other because.

With respect to claims 13-14, claim 6 of Patent (US 7,348,689) discloses the limitations of claim 13.

With respect to claim 15, claim 7 of Patent (US 7,348,689) discloses the limitations of claim 15.

With respect to claim 16, claim 8 of Patent (US 7,348,689) discloses the limitations of claim 16.

With respect to claims 13-14, claim 20 of Patent (US 7,348,689) discloses the limitations of claim 13.

With respect to claim 15, claim 21 of Patent (US 7,348,689) discloses the limitations of claim 15.

With respect to claim 16, claim 22 of Patent (US 7,348,689) discloses the limitations of claim 16.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARLOS AMAYA whose telephone number is (571) 272-8941. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

/C. A./
Examiner, Art Unit 2836